

THE FOLLOWING DTL-TTL COMPARISON DISCUSSION HAS BEEN REPRODUCED FROM THE DESIGN MANUAL OF DATA TECHNOLOGY CORPORATION.

2.3 CIRCUIT DETAIL

2.3.1 Characteristics

OPERATING PARAMETERS

Logic Levels

Logic "1"	+2.0 to +5.0 V
Logic "0"	0 to +0.45V

Noise Margin

Logic "1"	1.6V, typ.
Logic "0"	1.0V, typ.

Input Loading

	@ Logic "0"	@ Logic "1"
DTL Circuits ("d" Load)	-1.4mA, max.	5.0 μ A, max.
TTL Circuits ("t" Load)	-1.6mA, max.	40.0 μ A, max.

Output Drive Capability

	<u>"d" Loads</u>	<u>"t" Loads</u>
DTL NANDs	8	3*
DTL Power NANDs	25	22
DTL Flip Flops	12	3*
TTL NANDs & Flip Flops	11	10
TTL Power NANDs	34	30

Frequency Range **

DTL Circuits	DC to 5 MHz
TTL Circuits	DC to 20 MHz

Power

V_{CC} (Operating Voltages)	+5 V dc, +5%
$I_{CC A}$ (V_{CC} Current)	Specified/Module

NANDs: All Inputs High
 Flip Flops: Clock Pulse High
 Others: Maximum Value

$I_{CC B}$ (V_{CC} Current)	Specified/Module
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NANDs: All Inputs Low
 Flip Flops: Clock Pulse Low
 Others: Minimum Value

$I_{CC}(\text{typ})$ (V_{CC} Current) Specified/Module

Recommended value for specifying
 power supplies in typical system

* 6 "t" loads, when external collector resistor (3 kilohm returned to
 +5V is used.

** Unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS*

Power (V_{CC})

DTL	+8.0V dc, cont.
TTL	+7.0V dc, cont.

Temperature

Operating	0°C to +70°C
Storage	-55°C to +125°C

Inputs

DTL Logic "1"	+5.5V ⁺
Logic "0"	0V, min. [‡]
TTL Logic "1"	+5.5V
Logic "0"	0V, min.

Outputs **

NANDs & Flip Flops	30 mA
Power NANDs	100 mA

* Beyond which life of unit may be impaired

** Current Sink (into output)

+ Higher levels may be used if current limited to 1 mA

‡ Lower levels may be used if current limited to -10 mA

2.3.2 Diode Transistor Logic (DTL)

DTL's lines of digital modules are based on the DTL (930 Series) form of integrated circuits. The selection of this DTL circuitry was made after a complete and extensive analysis of the tradeoffs between speed, power, noise immunity, price, and availability of all the various forms of integrated circuits. Some of the outstanding advantages of using this popular type of integrated circuitry are:

a. Simplicity

- One power supply voltage (+5 volts). No off bias is required on circuits; power distribution is simplified and is reduced.
- Simple loading rules. Only one standard load (-1.4mA, max.) is required.
- NAND circuits. Simple logic manipulation is provided.

b. Versatility

- Node on Four-Input NANDs. There is easy expansion of inputs (higher fan-in) with the simple addition of diodes.
- Large collector resistance. Circuits can be wire-ORed (i.e. outputs of several NANDs can be tied together); up to ten of the basic NANDs can be paralleled.
- Master-Slave Flip Flop provides threshold switching. This eliminates the concern of amplitude and rise and fall times of the input clock pulses; there are no commutating or input coupling capacitors. The Master-Slave storage technique with the inhibit control of inputs during switching, eliminates any ambiguous or false triggering; further detail is provided in Section III, paragraph 3.1.3
- Buffered Flip Flop circuit eliminates collector triggering experienced with the discrete capacitively coupled circuits. The basic 945 Series DTL Flip Flop has built-in buffer stages which eliminate the susceptance to any noise spikes on the outputs.
- Direct Set and Clear override eliminates troublesome glitches on the output when clearing Flip Flops. The

Direct Set and Clear inputs on the Master-Slave Flip Flop completely override the clock pulse operation, giving clear positive control of any clearing or presetting operations.

- DTL is compatible with TTL circuits. The DTL (930 Series) integrated circuits provide the best interface of any other popular circuit; both circuits are current sinking (DTL = 1.4 mA, max.; TTL = 1.6 mA, max.) and have comparable input thresholds (typically 1.4 volts). Details on this interface and the compatibility of DTL and TTL is provided in paragraph 3.3.3
- DTL can interface with RTL. The basic DTL (930 Series) integrated circuits will drive the popular RTL integrated circuits, using the Power NAND or the basic circuits with external 500 ohm collector resistors to +5 volts.
- DTL can interface with Unclamped Discrete Circuits. When input signals exceed the maximum of +5.6 volts, a standard Four NAND circuit with Node can be used with discrete diode inputs to the Node. This prevents the input diode breakdown at 5.6 volts on the integrated circuit inputs.

c. Speed

- All DTL (930 Series) integrated circuits will operate up to 5 MHz with proper loading and wiring techniques.
- Basic NAND gate circuitry allows control of switching speed.
 - The large collector resistance (typically 6 kilohms) slows down turn-off time for minimized interference. The shunt load capacitance in wiring or by a discrete capacitor causes a slow ($RC \approx 6 \times 10^3 C$) through the collector resistance.
 - Faster turn-off (higher speed) can be obtained when necessary. A 3 kilohm to +5 Volts on the output gives typically a 3:1 improvement in turn-off time. Ref. pages 2-9 and 2-31 respectively show detail on the effects of shunt capacitance and pre-loaded outputs.

- Turn-on time of the NAND circuits can be decreased providing minimum interference for line transmission by the addition of capacitance to the node ($RC = 3.75 \times 10^3 C$). Section III shows graphs of this effect.

- Speed (turn-off time) improves when more loads are driven and shunt capacitance is minimized. The improvement comes from the addition of typically 3.75 kohms to +5 V when each active DTL circuit is driven. This is loading presented by the input of the typical DTL circuit until the input threshold is reached. The additional resistance to +5 V helps to charge the shunt capacitance in the turn-off condition. Paragraph 2.4.5 describes the effect of adding loads to the typical DTL circuit.

d. Noise Immunity

- A threshold of typically +1.4 V provides 0.75 to 1.2 V (typically 1.0 V) of noise margin in all inputs.
- The input threshold is more defined. The all semiconductor switching path (i.e., diodes and transistors) eliminates the broad linear area present in discrete circuits, where resistors were used to obtain biasing.
- Threshold (or dc) switching yields minimum susceptance to frequency of noise. Faster transistors and better design eliminate the necessity for speed-up or commutating capacitors. Even better rejection will be possible as the dielectrics and masking techniques used in fabrication of integrated circuits are improved.
- No unnecessary power is switched. The saturated output driving transistor does not switch power when turning on unless the circuit is loaded. The large collector resistance (typically 6 kohms) minimizes the current being switched and reduces noise in the power lines.

2.3.3 DTL-TTL Compatibility

a. Features. Both the Blue Chip and Black μ -Logic lines offer DTL and TTL modules. The DTL and TTL modules of each line are of the same physical characteristics and are pin-for-pin interchangeable for the simple gate and flip flop functions. This facility of using either

logic form allows the designer to optimize his system through the advantages offered by each*; the major trade offs being:

Speed

DTL	0 to 5 MHz
TTL	0 to 20 MHz

Performance

DTL	Gating Facility - Node Expansion, Wired "OR"
TTL	Multifunctions - Decade Counters, Adders, etc.

* Reference General Operating Parameters, page 2-8

b. Commonalities. The 930 Series DTL and 7400 Series TTL integrated circuit chips are used to implement the DTL and TTL modules for both the Blue and the Black Chip lines. The chips and resulting modules are compatible and exhibit the following basic commonalities:

Physical: IC Chips are housed in the dual inline 14-pin packages.

Electrical: One power supply, +5 V (+5%)

Signal: Logic "1" = +2.0 to +5.0 V
Logic "0" = 0.0 to +0.45 V
Threshold = 1.4V, nom.

Logic: NAND is basic logic function

Input: Current sinking mode of operation; current is absorbed by the driver circuit when the following input is in active state (i.e., low or Logic "0").

Drive: In the active state, the output is a saturated switch to ground which absorbs current from circuits being driven.

c. Interfacing. The basic definitions of the DTL standard load ("d" load) and the TTL standard load ("t" load) are provided in the General Operating Parameters, Section 2.3.1. It will be noted from these definitions on input loading, that when interfacing DTL and TTL circuits, there is very little difference in the current sinking required for a Logic "0", i.e., the basic "d" load is -1.4 mA and the

basic "t" load is -1.6 mA. However, there is an appreciable difference in the leakage to be supplied when the input is at a Logic "1"; i.e., the basic "d" load has a reverse leakage of 5 μ -amps and "t" load has a reverse leakage of 40 μ -amps. This difference of leakage becomes the controlling factor when interfacing the DTL and TTL circuits. A synopsis of performance characteristics for the DTL and TTL modules is given in the tabulation of the Logic Module Brochure, Section X. This brochure delineates the typical performance to be expected from the respective modules and the fan-in and fan-out in terms of DTL ("d" loads) or TTL ("t" loads) circuits. When using both DTL and TTL circuits, it may be helpful to observe the following rules:

- Never drive more than three TTL circuits from the basic DTL NAND or Flip Flop (circuits using the 087, 088, or 089 integrated circuit chips) without adding an additional 3 kohm to +5 V; this connection will allow 6 "t" loads to be driven. This does not apply to the Power NAND circuits (i.e., all circuits using the 086 chip). Refer to the write-up on each chip, Section III, or the easy-to-use listing in the Logic Module Brochure, Section X, for details of fan-out between DTL and TTL circuits.
- Never wire-OR two TTL circuits or a DTL and TTL circuit; only the basic DTL NANDs and Flip Flops (circuits using the 087, 088, or 089 integrated circuit chips) can be wire-ORed.
- Pay particular attention to the handling of signal lines to minimize noise pickup. This and other pointers will be covered by a detailed write-up in Section VII, DATA TECHNIQUES.

2.3.4 Transistor Transistor Logic (TTL)

The Transistor-Transistor form of integrated circuit has become increasingly popular with the increase in the number of manufacturers, advertising, and the lowering of prices. At first, the TTL integrated circuits suffered from lack of standardization; there existed no common pin or circuit arrangement such as that established early in the DTL integrated circuits (the 930 Series). However, with the advent of the less expensive dual inline packaging and the inherent high yield in the manufacturing, this form of logic has come down in price to compete with that of the higher volume 930 Series, DTL circuits. The use of these circuits has been further enhanced by the effort on the part of some manufacturers to build pin-for-pin compatible TTL and 930 Series DTL circuits; Texas Instruments Company has been a leader in this area offering its pin-for-pin 7400 N series TTL. There are pros and cons to the use of the higher speed TTL circuits; some of these are listed below. These points have been prepared with the Texas Instruments Company 7400 N series TTL circuits in mind; minor differences may exist when contrasted with other forms of TTL circuits.

a. Advantages.

- The TTL propagation delays of 8 to 15 nsec (typically 11 nsec) are almost three to one better than the DTL (typically 30 nsec). This improvement is a result of two basic TTL circuit characteristics.

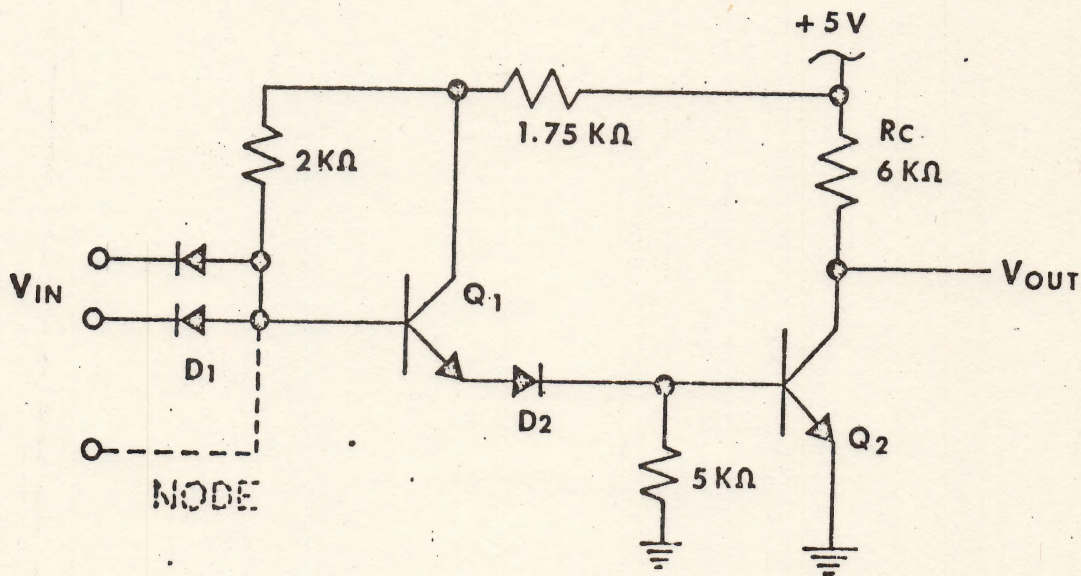


Figure 2-3 Typical DTL Circuit (930 Series)

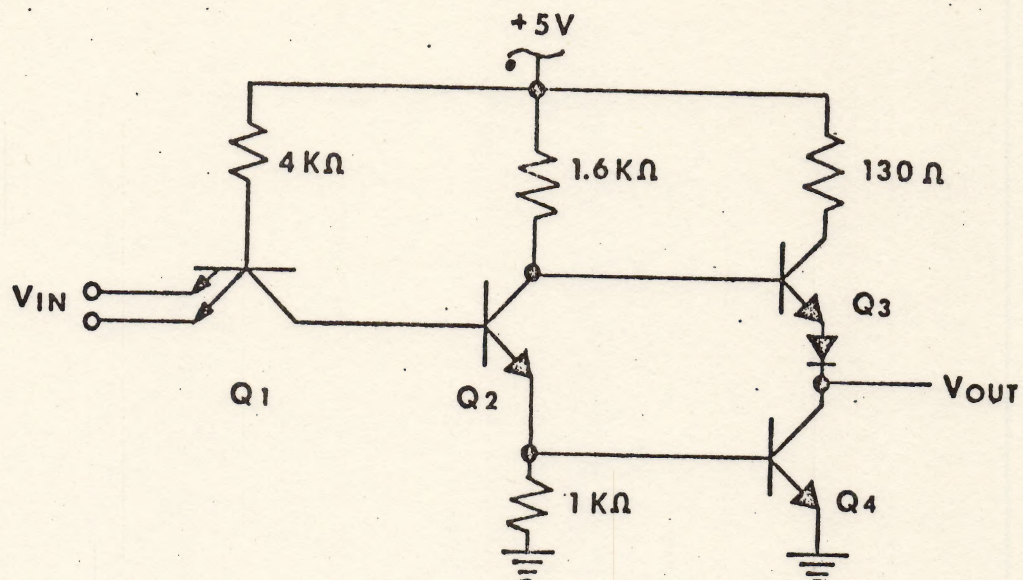


Figure 2-4 Typical TTL Circuit (7400 Series)

- Active pull-up. Figures 2-3 and 2-4 show a typical TTL and DTL circuit. The TTL circuit has a transistor (Q_3) in place of R_C in the DTL circuit. This transistor is switched on when the shunt transistor (Q_4) is turned off and the output is going positive to $+V_{CC}$. This form of output gives an impedance of typically 70 ohms to charge the shunt load capacity; in contrast with the typical 6 kohms of the 930 Series DTL. This transistor (the active pull-up) provides the difference in the turn-off time of the TTL and DTL circuits (typically 18 and 45 nsecs. respectively).
- Multi-emitter input. Only transistor junctions are involved in the switching path of the TTL circuits. Figure 2-3 and 2-4 show the typical DTL and TTL circuit with their respective diode and multi-emitter inputs. Although equivalent thresholds are achieved because of an equal number of semiconductor junctions, the

higher speed operation of the multi-emitter transistor input yields a faster turn on time for the TTL circuit (8 nsec versus 25 nsec, typical for DTL circuits).

- Multi-functions (or large arrays) that are not possible with the DTL circuits are more readily obtained using the TTL circuit techniques. The simpler masking and higher yields are largely responsible for the advances made in the large scale integration with the TTL circuits. TTL circuits will perform over wide deviations in the basic parameters. Because of this advantage, it is expected that most of the practical advances in large scale integration will be made using this technique for at least the next two years; until the inherent problems of the Metal Oxide Silicon (MOS) technology are solved and this form of logic becomes practical.

b. Disadvantages

- In systems using TTL circuits particular attention must be directed to minimizing noise. The faster response and resulting switching speeds of these circuits makes them generate and respond to more noise than their DTL counterparts. Some important facts about TTL circuits are:
 - Noise Margins. Both TTL and DTL exhibit noise margins in the area of 1.0 V. Integrated circuit manufacturers do not provide any detail information on the noise immunity of integrated circuits with respect to frequency. But when all the junction and parasitic capacitances are considered, there exists a frequency dependence on the performance of integrated circuits as with diodes and transistors. With the higher frequency response of the TTL circuits, it is only natural that they will respond and be more sensitive to higher frequency noise than the DTL circuits.
 - Active Pull up Causes Current Surges. It is common knowledge that the additional transistor in the output of the TTL circuits causes noise on the +5 V and the ground return because both output transistors can be ON simultaneously. Figure 2-4 shows that if transistors Q_3 and Q_4 are on together, a current surge in excess of 30 mA can be drawn from the +5 V and put into the ground bus. These spikes will be of from 10 to 20 nsec wide,

and although generally limited by the use of decoupling capacitors on the +5 V, they may still appear on the power distribution system.

- Induced Noise. With the higher speed characteristics of TTL circuitry, both current and voltage induced noise are present.

Current induced noise is a problem when large currents are switched at high speeds. Any signal line carrying high current transients can couple noise into adjacent signal lines through their mutual inductive coupling. All adjacent lines have some mutual inductance, and at high di/dt transients, this will form an effective inductive coupling to couple current noise spikes. Noise coupling of this type can be minimized by using twisted pair and limiting high current transients. When high current surges are pulled from the V_{CC} and dumped into the ground return, voltage drops occur from the series inductive reactance. These voltage drops are controlled by using low reactance power bus (such as laminated bus) and by minimizing fast current switching.

Voltage induced noise is generated when fast transitions occur with relatively high impedance lines. All adjacent wiring has some mutual capacitance and this capacitance will differentiate and couple spikes to the adjacent lines from any line with fast voltage transients. This coupling is minimized if lines are short with low impedances, and if fast voltage transients are minimized, or if twisted pair is used.

- Although the TTL technology will provide the more complex functions and multi-arrays of the future, the basic circuits have certain performance limitations.
 - No wired-OR. This ability to tie outputs of the NAND circuits together is a powerful feature of DTL circuits; it cannot be implemented with the TTL circuits because of the active pull-up transistor and the resultant low impedance drive.
 - Limited Fan-In. TTL circuits cannot be expanded because of their sophisticated multi-emitter input con-

struction, except by the addition of other multi-emitter input circuitry. Expansion in this fashion provides an AND-OR operation where the AND of each multi-emitter construction is ORed by the output stage of the basic gate. This is not as useful as the diode expansion possible with DTL circuits which permits the formation of high fan-in NAND gates. Since the TTL circuits do not have the full NAND expansion capability, any large NAND gate requirements must be anticipated and covered with large multi-emitter circuits; hence, the 6, 8, and 10 input TTL circuits available from more manufacturers.

- Poor Short Circuit Immunity. The active pull-up transistor of TTL circuits makes them susceptible to damage when outputs are shorted to ground for extended periods. Although designed for beta and current limiting, deviations in deposition of resistors and transistors from batch to batch makes them vulnerable to damage.

2.4 BASIC PARAMETERS (Defined and Discussed)

2.4.1 Standard Load

The rule for establishing the number of circuits of a particular type that can be driven from another circuit are simplified by defining a "standard load". A standard load is that load seen by the driving circuit when connected to one input of a two input NAND gate or its equivalent. DTC uses both the DTL and the TTL Integrated Circuits for its Blue Chip and Black μ -Logic modules. Therefore, a standard load will be defined for both. The input and output loading (fan-in and fan-out) for each DTL and TTL circuit in the Blue and Black module line is provided in Section X. These loads are specified respectively in the "d" and "t" loads as defined in the following:

a. DTL

- The conventional definition for the standard load of a DTL circuit is that of specifying the maximum current drawn by a driving circuit when the output is low. Figure 2-5 shows that for a low output ($V \leq +0.45V \approx 0.0V$) the driving circuit will pull a maximum of 1.4 mA (1.15 mA typical). This current pulled by the driving circuit defines a unit or standard load in a conventional sense.

This is true because a DTL circuit is a current sinking form of logic and the current pulled in the low state is generally the limiting factor on the number of circuits which can be driven (fan-out).

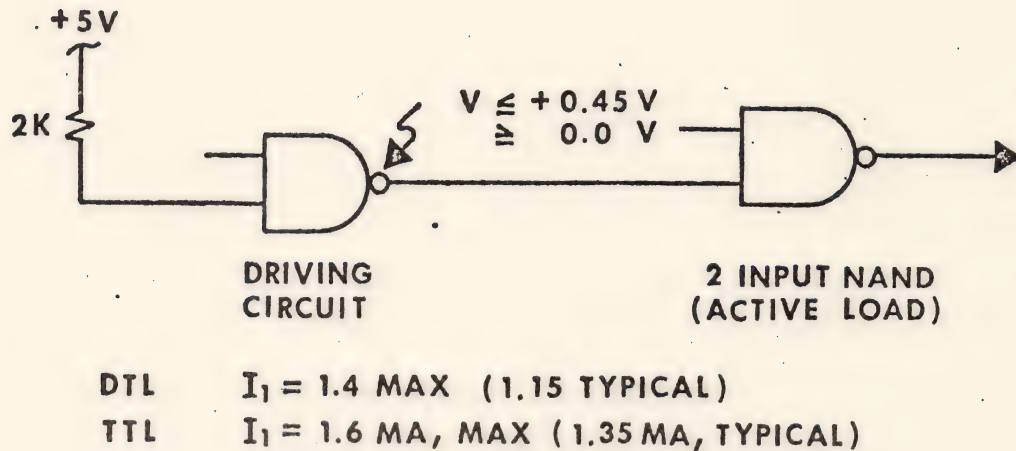


Figure 2-5 Standard Load (Low Level)

- When the output of the driving circuit is at a high level (+2.0 to +5.0 V) the diodes on the input of the circuit being driven are back biased. Therefore, only a nominal 2-5 μA are drawn by the circuit being driven. This is shown in Figure 2-6 where current I_1 is the leakage current when the driving circuit is at the high level. Since this leakage current is so low, it is seldom the limiting factor upon the number of circuits being driven, and is quite often not even mentioned in specifying the fan-in and fan-out of the DTL circuits.

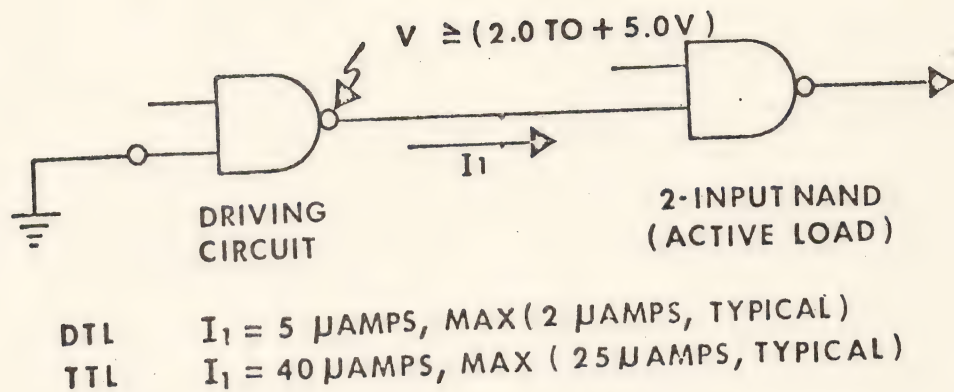


Figure 2-6 Standard Load (High Level)

b. TTL

- The standard load for the TTL circuits are very similar to those for the DTL circuits. The current drawn by the driving circuit when in the low logic level ($V \leq +0.45V$, $\geq 0.0V$) is 1.6 mA maximum, (1.35 mA typical). Just as with the DTL logic, the TTL logic is also of a current sinking operation. Therefore, this 1.6 mA maximum current generally defines the unit or standard load and is the limiting factor when specifying input and output driving requirements.
- With the TTL form of logic, the leakage current pulled by the circuit being driven when the driving circuit is at the high level (+2.4V, minimum), is 40 μA maximum (25 μA typical). This is considerably larger than that of the DTL circuits and is a limiting factor on fan-out when TTL circuits are being driven from the 930 Series DTL circuits. This effect can be seen in the fan-out specifications for each module refer to Section III, IC Chips, or in the easy reference brochure, Section X.

2.4.2 Fan-In and Fan-Out

Although the input and output characteristics of the DTL and TTL circuits are generally expressed in terms of the standard load, it must be understood that certain other parameters may very well dictate the fan-in or fan-out of circuits.

a. DTL

- The DTL, 930 Series, integrated circuits, because of their 6 kohm collector output resistance, are susceptible to load capacitance. The load capacitance presents itself in the output wiring and in the diodes of the circuits being driven. Generally, one should figure on 2-3 pF of capacitance per DTL input and approximately 15 to 20 pF of capacitance per foot of interconnect wiring. The capacitance of the wiring varies with how random the interconnect is and whether lacing is employed. Reference to Section III, IC Chips, will show that a plot of Turn-Off Time vs. Load Capacitance as provided on all of the DTL integrated circuits.
- Only the DTL circuits have the ease of increasing fan-in by the addition of diodes to the node. The four input NAND with node and the four input Power NAND with node are the most common DTL circuits exhibiting the node for increasing fan-in. It should be noted that the addition of diodes to the node of a circuit degrades the turn-on time. When using the node for expansion, one should figure approximately 2-3 pF per diode and 15 to 20 pF per each foot of interconnect wiring. The affect of node capacity on the performance of the circuits can be seen by the graphs of Turn-On Time vs. Node Capacity provided for the Dual 4 NAND/node chip (Model 088) and the Dual 4 Power NAND/node chip (Model 086) provided in Section III, IC Chips.

b. TTL

- The TTL circuits, because of their active transistor pull-up, show very little susceptance to load capacitance. Therefore, curves showing degradation in turn-off or turn-on are seldom provided for the TTL circuits.
- The TTL circuits do not have the facility of input expansion.

sion (fan-in) by the simple addition of diodes, the effect of node capacity does not show up with the TTL circuits. However, some special versions of the TTL circuitry do allow the AND-OR operation by the addition of multi-emitter structures to the input. These circuits, when used, exhibit the same degradation in speed when capacitance is added to the expansion nodes.

2.4.3 Logic Levels and Noise Margin

a. Typical Operation. The operating logic levels for both DTL and TTL circuits are comparable and as a result, they are completely compatible with each other. Typical values of logic levels and thresholds are shown in Figure 2-7. The shaded areas represent the Logic "1" and Logic "0" ranges of the outputs from DTL and TTL circuits; the threshold levels represent the input characteristics of the circuit being driven. The values of noise margin are shown to be 1.6V from a Logic "1" and 1.0V from a Logic "0"; these values are quite typical and can be expected in normal operation.

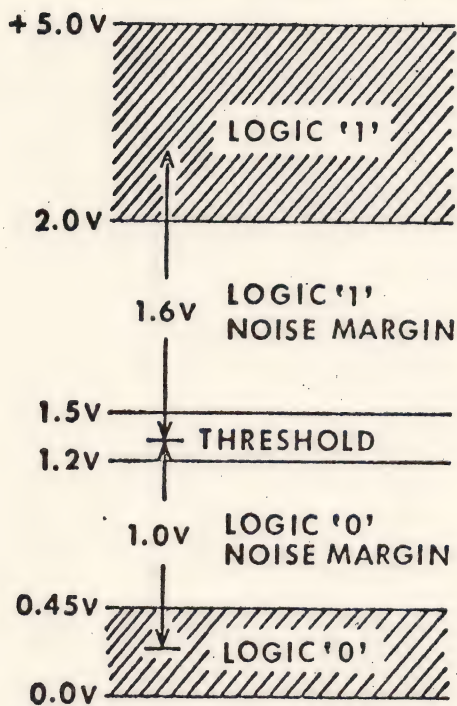


FIGURE 2-7
TYPICAL LOGIC LEVELS
(NOISE MARGINS)

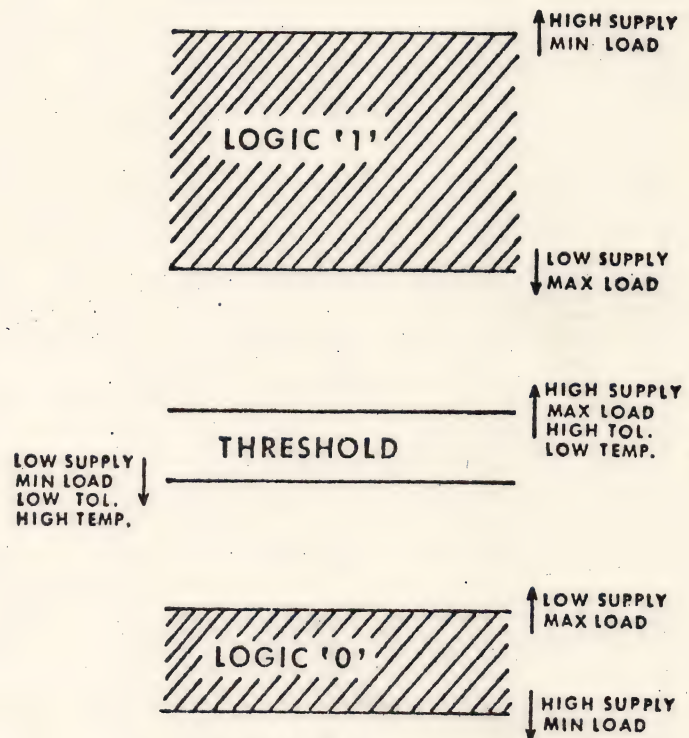


FIGURE 2-8
FACTOR AFFECTING LOGIC LEVELS

b. Worst Case Operation. The logic levels and threshold values shown are functions of such factors as loading, power supply level, temperature, and unit-to-unit tolerances; the relative effects of these factors are shown in the preceding illustration Figure 2-8. The end values of these various effects are difficult to correlate between the 930 DTL and the 7400 TTL because of differences in test conditions and means of specification used by the various integrated circuit manufacturers. As an example, the 7400 Series is actually tested to give a guaranteed DC noise margin of 400 mV at full load, low power supply voltage, and throughout its entire operating temperature range. On the other hand, the 930 Series is usually tested at normal power supply voltages, room temperature, and worst case loads. When the data is studied, however, a good correlation is obtained and the aforementioned values are highly useful and realistic design values.

c. Frequency Dependence. The values of noise margin, either typical or guaranteed, are always specified as the DC noise margin; however, the noise margin is frequency dependent. The user is required to use refinement in his design and construction techniques to eliminate possible sources of high frequency noise. Several good articles have been written on minimizing the effects of noise; some of this data will be available in Section VII DATA TECHniques and in the Appendix, Section X.

2.4.4 Measurement

a. Definitions: With the introduction of integrated circuits, the measurement and specifications associated with digital logic circuits have changed. The discrete logic circuits employed speed-up capacitors commutating capacitors, and other AC coupling. Therefore, the discrete logic circuits were very dependent upon the characteristics of their input signals. The amplitude, rise time and fall time had to be specified and performance was predicated on a guaranteed rise and fall time with a minimum change in amplitude. This was necessary to couple energy through the capacitors employed for the higher speed operation. With integrated circuits, the means of specifying and measuring performance characteristics changed from rise and fall times with minimum amplitude to turn-on and turn-off times with respect to passing through an input threshold of nominally 1.5 V. Use of the 1.5 V point has become an industry standard; it is above the nominal 1.4 V threshold point and provides certainty that the circuit has switched. Since the DTL and TTL circuits are all direct coupled, all circuit will switch when the input threshold of the circuit being driven is reached. Therefore, the performance of the circuits are specified using the turn-on and turn-off times as described.

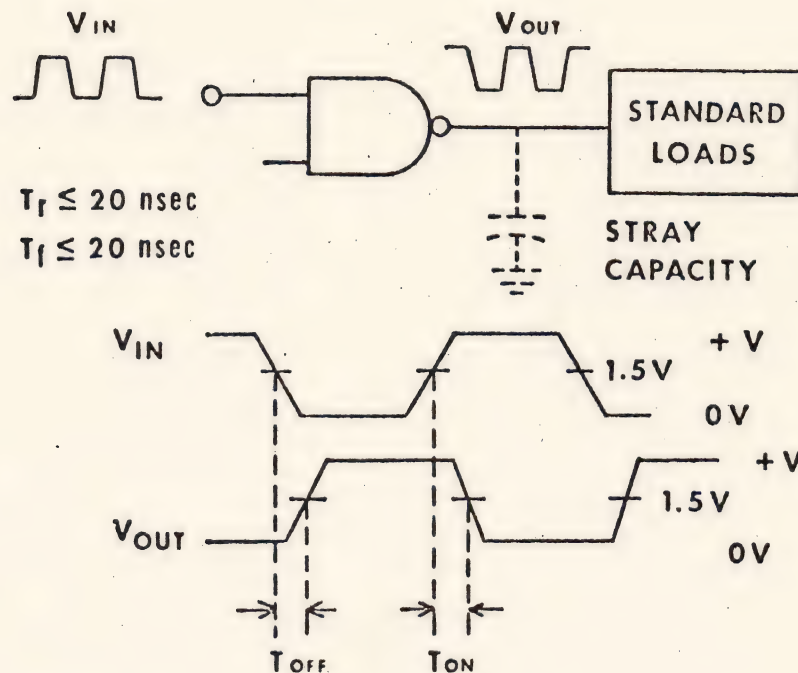


Figure 2-9 Typical Measurements (Turn-On and Turn-Off)

b. Application. Figure 2-9 shows a typical turn-on and turn-off measurement with the 2 NAND circuit and is of that normally used to test the DTL and TTL circuits for propagation delay $\left(\frac{\text{Turn-on time} + \text{Turn-off time}}{2} \right)$ and logic levels under load conditions. The circuit under test is driven from a pulse source with good rise and fall times and the circuit is loaded with active circuit inputs and shunt capacity (to simulate the capacitance in wiring and in the inputs of the circuits being driven). The wave forms in Figure 2-9 show that the turn-on time and turn-off time are measured with respect to the 1.5 V the input and output signal respectively. As previously explained, these turn-on and turn-off times are the figures used in specifying the performance of the DTL and TTL integrated circuits.

typical DTL integrated circuit. The diode input shown in Figure 2-10 simulates the input diode to the typical DTL circuit and provides, along with the 2.1 V allotted for internal junctions, for nominal 1.4 V input threshold. We can see that when the input voltage to this circuit reaches the nominal 1.4 V level, the input diode becomes back biased and simulates the turning on of the conventional DTL integrated circuit. The stray capacitance shown in the figure is that generally used to simulate the wiring and input capacity associated with loading. This capacitance is generally a discrete capacitor (such as 47 pF) when a load simulation circuit of this nature is used for testing.

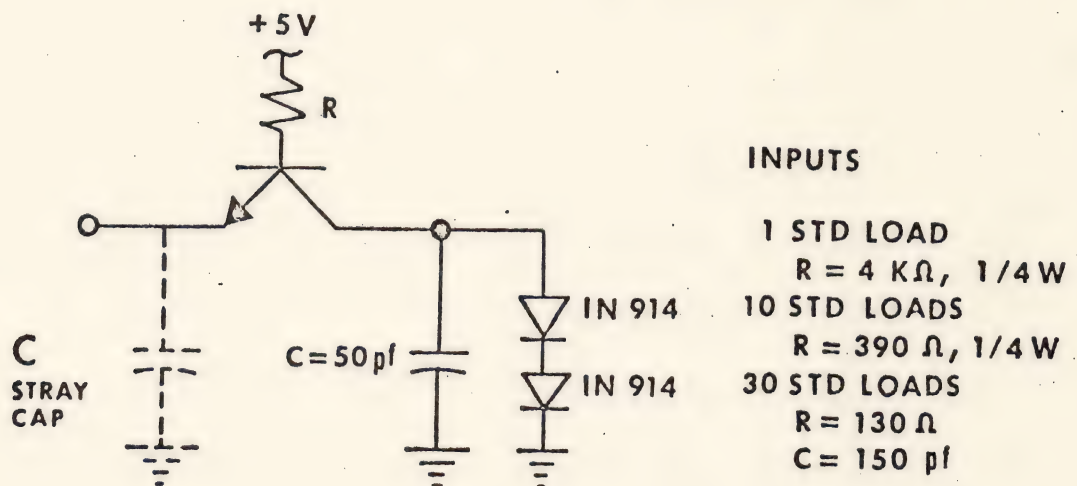


Figure 2-11 TTL Standard Load Simulation

- The TTL standard load simulation circuit, shown in Figure 2-11, is that generally used for testing propagation delay and logic levels for TTL integrated circuits. The two diodes shown in shunt to ground provide simulation of the semiconductor junctions (0.7 V nominal, per junction) which is seen in the conventional TTL circuit. The transistor shown in Figure 2-11 simulates the multi-emitter transistor seen on the conventional TTL circuits. The

linear (unsaturated) operation of transistors in the TTL circuitry makes it more difficult to show the exact derivation of the input threshold. However, it can be seen from Figure 2-11 that when the emitter input becomes back biased at a nominal threshold of 1.4 V, the input transistor cuts off and simulates the turning on of the conventional TTL circuit. Figure 2-11 shows a shunt capacity of 50 pF; this is the capacitance associated with the junctions internal to the integrated TTL circuitry. The stray capacitance shown on the emitter of the input transistor is that associated with the wiring and input junctions. This capacitance is generally simulated by a discrete value (typically 50 to 100 pF) and is specified for the test being conducted. The input loading (current sinking load) is controlled by varying the value of R. Typical values for the respective standard loads is shown in the figures; note that full loads for the basic TTL circuits (10 standard loads) and the power NANDs (30 standard loads) are covered by the table.

2.4.5 Waveform Characteristics

a. DTL

The output waveform characteristics of integrated circuits disturbs the first-time user of integrated circuits. Figure 2-12 shows a typical waveform characteristic for the DTL integrated circuits. The input and output waveforms are judged on their performance with respect to the 1.5 V point. A glance at the wave form on the output shows that above 1.5 V the waveform has a very slow recovery. Since the DTL integrated circuits are not sensitive to the rise and fall times, once the threshold has been reached on an input that circuit turns on and in this manner the intelligence of a digital system built with integrated circuits propagates at the threshold level. Recovery time above the threshold point is of no concern.

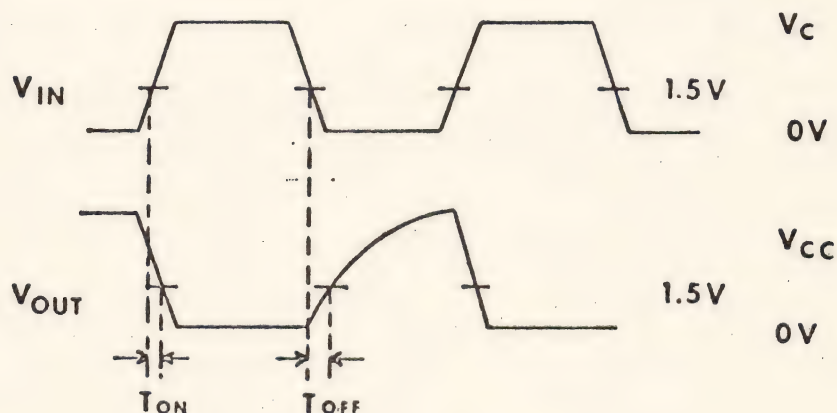


Figure 2-12 Typical Waveform Characteristics DTL (930 Series)

- The slow recovery of the DTL circuits when the output transistor is turning off, is caused by the 6 kohm output collector resistance of the typical DTL circuit (Figure 2-3). This 6 kohm resistance must drive all the shunt capacity associated with each load. However, with the DTL circuitry a very unusual thing happens: the 6 kohm output impedance of the driving circuit is aided in charging this shunt capacity towards the threshold point by the addition of each standard load. Figure 2-10 shows the equivalent circuit for simulating inputs; from this, it can be seen that up until the input diode becomes back biased, the typical DTL circuit provides a parallel resistance of 3.75 kohm to +5V (for each standard load). This parallel resistance of helps to charge the shunt capacity and therefore improves the turn-off time. Therefore, we get an improvement in performance of the DTL circuit with the addition of loads. This is compromised, of course, by the amount of shunt capacity added, particularly in the wiring. Figure 2-13 shows a typical plot of Turn-off Time vs. Load Capacitance for different load conditions on the typical NAND and Power NAND. The effect of load capacity with the Power NAND, of course, is not as noticeable, since this circuit uses an active pull-up instead of the 6 kohm collector resistance.

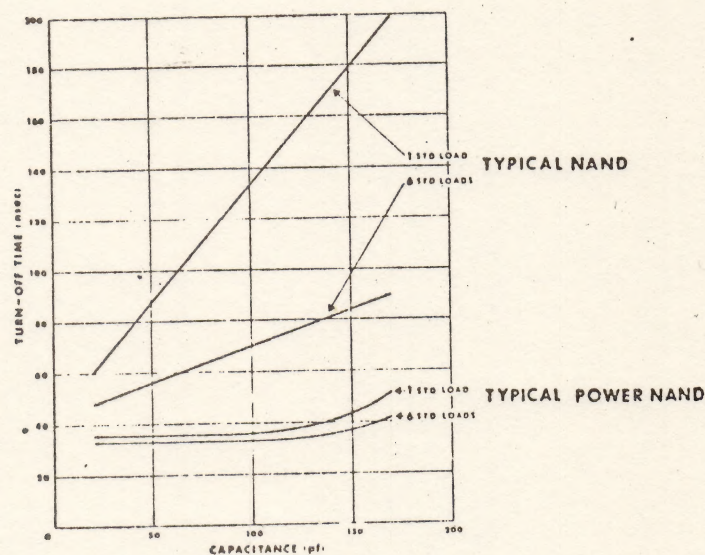


Figure 2-13 Turn-Off Time vs. Load Capacitance DTL (930 Series)

- Figure 2-14 shows a detail of the effect of loading on the turn-off time of the typical DTL circuits. The output waveform, curve A, would be typical of the expected turn-off time for one standard load and a nominal amount of shunt load capacity. Curve B would be the performance expected with the addition of three standard loads; note that there is a significant improvement in the turn-off time up to the 1.5 V point. Above this, the added standard loads have their input diodes back biased, and all the shunt load capacitance is being charged by the driving circuit's $6K\Omega$ collector resistance. Therefore, there is no improvement in the rise time above the threshold point of the circuits being driven. Curve C of Figure 2-14 has been drawn to show the effect of pre-loading the driving collector circuit with a resistor. This curve shows that a significant improvement has been gained in the turn-off and in the entire rise time of the output pulse. This can be done any time the designer requires higher speed operation and is willing to sacrifice some fan-out (that is current sinking capability) on the driving circuit. This would be the type of performance expected if a $3K\Omega$ resistor was tied to +5V (yielding an effective $2K\Omega$ collector resistance) on the driving circuit.

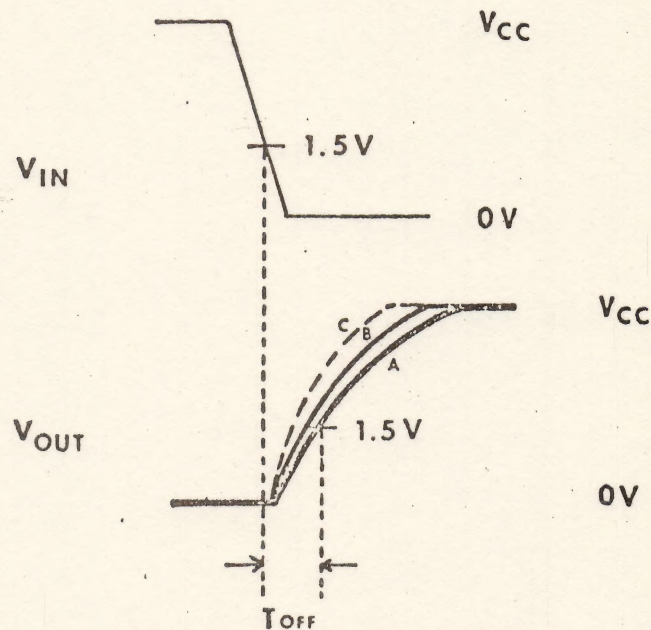


Figure 2-14 Effects of Loading on Turn-Off Time DTL (930 Series)

- Table 2-2 shows the typical turn-off times to be expected when the collector of a driving circuit is pre-loaded with a discrete resistor to +5V. This table also shows the standard loads which must be subtracted from the fan-out of the circuit to which the pre-loaded resistor is connected; note that the table gives the turn-off time expected with two different values of shunt capacitance.

Value of shunt resistor	std D load equivalent	TURN-OFF TIME	
		C=47 pf	C=100 pf
Open	0 std loads	105 nsec	210 nsec
3.6 K	1 std loads	42 nsec	84 nsec
1.8 K	2 std loads	25 nsec	53 nsec
1.2 K	3 std loads	25 nsec	39 nsec
910 ohm	4 std loads	25 nsec	30 nsec
750 ohm	5 std loads	25 nsec	25 nsec
620 ohm	6 std loads	25 nsec	25 nsec
560 ohm	7 std loads	25 nsec	25 nsec
470 ohm	8 std loads	25 nsec	25 nsec
430 ohm	9 std loads	25 nsec	25 nsec
390 ohm	10 std loads	25 nsec	25 nsec
360 ohm	11 std loads	25 nsec	25 nsec
330 ohm	12 std loads	25 nsec	25 nsec

Table 2-2 Turn-Off with Pre-Loaded Collector
DTL(930 series)

- With DTL integrated circuits certain gates are provided with a node. Discrete diodes can be added to this node in parallel with the conventional diode inputs, to provide higher input gates. The addition of diodes and the associated wiring, adds shunt capacity to this area of the circuit. Figure 2-3 shows that the node of the typical DTL circuit is located at the base of the input transistor. Any shunt capacity added to the node must be charged before the circuit can turn-on. Therefore, when adding diodes and wiring to the node of the DTL circuits care must be exercised to minimize the amount of shunt capacitance. The shunt capacitance will increase the turn-on time of the circuit since this capacitance must charge to the turn-on point of the gate through typically 3.75 K Ω to +5V. It can be seen that the limitation on fan-in to a circuit with a node is largely predicated on the amount of shunt capacity and the degradation in turn-on time for the particular application. Manufacturers typically provide a plot of node capacitance vs. turn-on-time for circuits which have a node. Graphs of this type are provided in Section III, I.C. Chips, for the Dual 4-Input NAND/Node chip and the Dual 4-Input Power NAND/Node chip.

b. TTL

The above discussion on the effects of shunt capacity have been those associated with the typical DTL circuits. The typical TTL circuit, Figure 2-4, has an active pull-up transistor instead of the passive 6 kohm of the DTL circuit. This active pull-up transistor makes the TTL circuit better able to drive shunt loading capacitance.

- With TTL circuits the effect of load capacitance is of no major concern, and performance characteristics of Turn-off Time vs. Load Capacitance are never given. The manufacturers generally state propagation delays (turn-on and turn-off times) with typical shunt capacitances; there is only a nominal difference between light and heavy shunt capacitance.
- TTL circuits, because of their sophisticated multi-emitter input do not have circuits with the node as that provided by the DTL circuits. Certain TTL chips do, however, have the ability to parallel the multi-emitter structure and provide an AND/OR type of operation. When additional multi-emitter structures are added to a gate of this type, these gates exhibit the same type degradation in turn-on time as that described for the DTL circuits. Detail information and plots of the nature provided for the DTL node capacity, are generally not provided for the TTL circuits.